PATENT ABSTRACTS OF JAPAN

(11) Publication number:

56-162858

(43) Date of publication of application: 15.12.1981

(51)Int.Cl.

H01L 27/04 H01L 29/72

(21)Application number : 55-066622

(71)Applicant : NEC CORP

(22)Date of filing:

20.05.1980

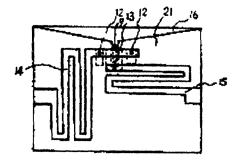
(72)Inventor: KUSHIYAMA TOSHIO

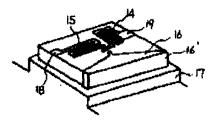
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To form an input/output matching circuit in a chip in response to the ground type by eliminating the influence of a parasitic inductance by the electrode pattern formed through an insulating film on a semiconductor chip.

CONSTITUTION: After the junctions of amplifying transistors used in emitter-(or base-) grounded type are formed, electrodes (designated by broken lines) are formed on the respective contacting regions. Then, an insulating film 21 is formed by a CVD or the like on the contacting electrodes, windows 19, 9, 12 are then opened at the base and the emitter as well as the collector and the contact electrodes, and electrode wiring patterns 14~16 are formed on the film 21. The patterns





14, 15 will become thereafter microstrip line type circuits. A semiconductor chip is soldered to the ground conductor 17 of a container, and the pattern 16 is grounded to the grounded conductor 17 via a ribbon-shaped conductor 16' or the like. The electrode pads 19, 18 of the strip line 14, 15 are connected to the external terminal of the container via a fine metallic wires.

LEGAL STATUS

[Date of request for examination]